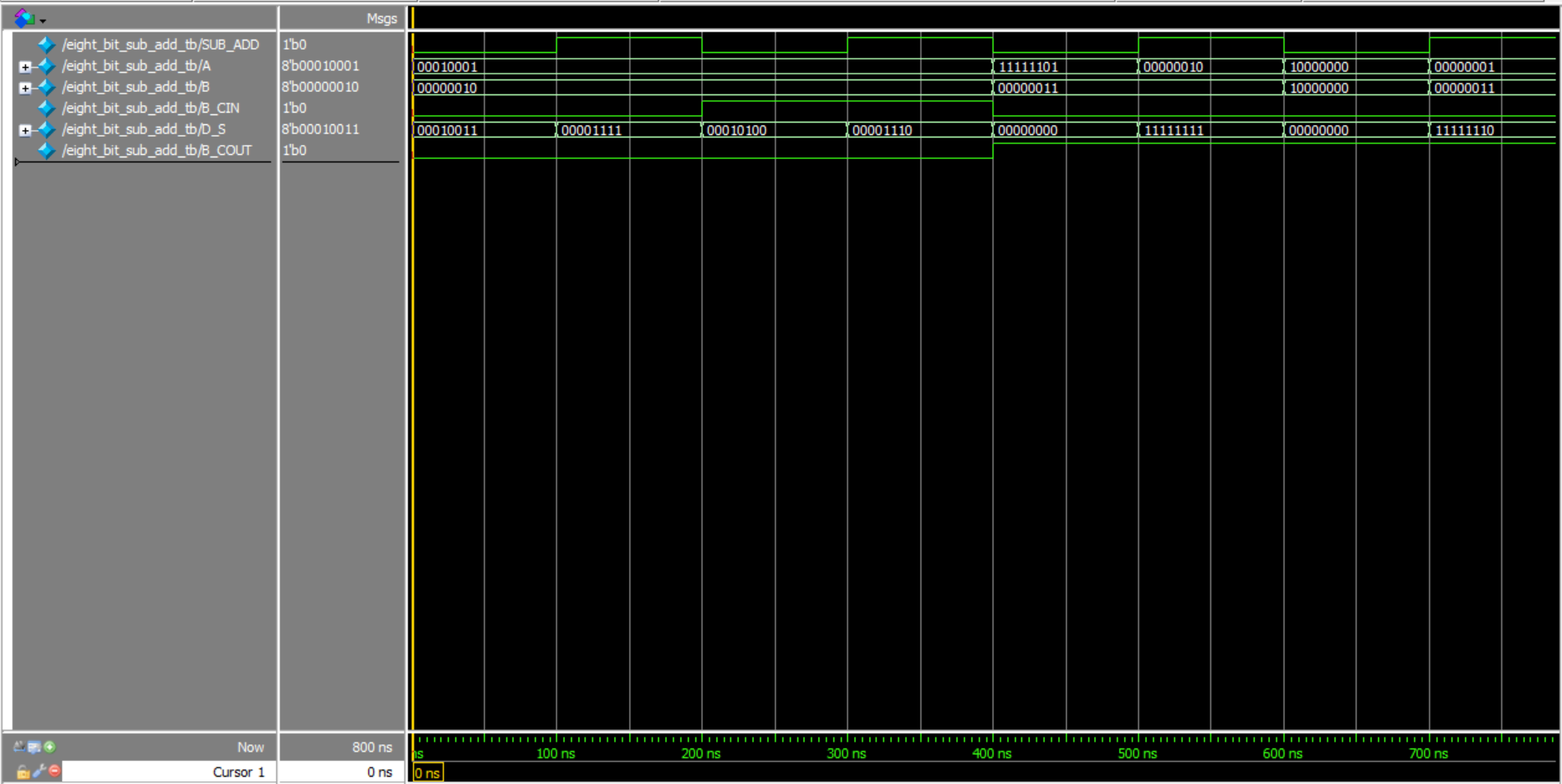
CPE 322 Simulation 1

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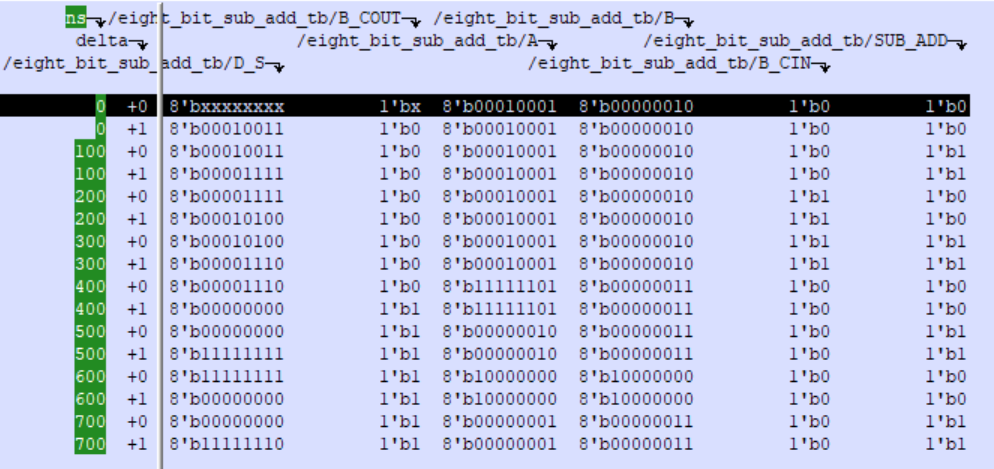
The file **eight\_bit\_sub\_add\_tb.v** contains the associated Verilog testbench. Below are screenshots of the waveform display and textual listing file outputs for the simulation for the period of time that the simulation was valid, in this case 800ns: 100ns for each of 8 test cases.

Starting from time zero, every 100ns interval, the next operation is performed, altering the values at each and maintaining them until the next interval mark as seen in Figure 1.



**Figure 1.** Waveform Output

On the time delta 0 of every 100ns interval, the inputs are loaded. Then, the outputs are calculated and loaded on time delta 1 for the same timestamp as seen in Figure 2.



**Figure 2.** Textual Listing Output

**eight\_bit\_sub\_add\_tb.v**

| // Eight-Bit Sub/Add Test Bench  `timescale 1ns/100ps  module eight\_bit\_sub\_add\_tb;  // internal wires and register declarations  wire [7:0] D\_S;  wire B\_COUT;  reg [7:0] A,B;  reg B\_CIN, SUB\_ADD;  // unit under test  eight\_bit\_sub\_add UUT (.D\_S(D\_S), .B\_COUT(B\_COUT),  .A(A),.B(B), .B\_CIN(B\_CIN),.SUB\_ADD(SUB\_ADD));  initial  begin  // 1) Add no carry on B\_COUT  SUB\_ADD = 0; // Add mode  B\_CIN = 0; // No Carry in  A = 17; // A = 8'b00010001  B = 2; // B = 8'b00000010  // D\_S = A + B = 19 -- 8'b00010011  // 2) Subtract no borrrow on B\_COUT  #100 // 100ns delay  SUB\_ADD = 1; // Subtract mode  B\_CIN = 0; // No Borrow in  A = 17; // A = 8'b00010001  B = 2; // B = 8'b00000010  // D\_S = A - B = 15 -- 8'b00001111  // 3) Add with pending carry on B\_CIN  #100 // 100ns delay  SUB\_ADD = 0; // Add mode  B\_CIN = 1; // Carry in  A = 17; // A = 8'b00010001  B = 2; // B = 8'b00000010  // D\_S = A + B + B\_CIN = 20 -- 8'b00010100  // 4) Subtract with pending borrow on B\_CIN  #100 // 100ns delay  SUB\_ADD = 1; // Subtract mode  B\_CIN = 1; // Borrow in  A = 17; // A = 8'b00010001  B = 2; // B = 8'b00000010  // D\_S = A - B - B\_CIN = 14 -- 8'b00001110  // 5) Add where internal carry propagates from LSB to B\_COUT  #100 // 100ns delay  SUB\_ADD = 0; // Add mode  B\_CIN = 0; // No Carry in  A = 253; // A = 8'b11111101  B = 3; // B = 8'b00000010  // D\_S = A + B = 256 -- 8'b00000000, B\_COUT = 1  // 6) Subtract where borrow propagates from LSB to borrow request on B\_COUT  #100 // 100ns delay  SUB\_ADD = 1; // Subtract mode  B\_CIN = 0; // Borrow in  A = 2; // A = 8'b00000010  B = 3; // B = 8'b00000011  // D\_S = A - B = -1 -- 8'b11111111, B\_COUT = 1  // 7) Add that causes an overflow into the carry bit  #100 // 100ns delay  SUB\_ADD = 0; // Add mode  B\_CIN = 0; // No Carry in the input from a previous stage  A = 128; // A = 8'b10000000  B = 128; // B = 8'b10000000  // D\_S = A + B = 256 -- 8'b00000000, B\_COUT = 1  // 8) Subtract larger positive number from smaller positive number  #100 // 100ns delay  SUB\_ADD = 1; // Subtract mode  B\_CIN = 0; // No Borrow in the input from a previous stage  A = 1; // A = 8'b00000001  B = 3; // B = 8'b00000011  // D\_S = A - B = -2 -- 8'b11111110, B\_COUT = 1  end  endmodule |
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